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Application Number	10/751,172
Filing Date	12-30-2003
First Named Inventor	Jae-Won HAN
Art Unit	2812
Examiner Name	Nguyen, Ha T.
Attorney Docket Number	OPP031047US

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10-31-5

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PTO/SB/08B (07-05)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known

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Sheet 2 of 2

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite. No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
lm	DA	Office Action dated May 21, 2005; Korean Patent Application No. 10-2003-0021958	
lm	DB	Hiroshi ABE, Masayasu SUZUKI and Shinichi ISHIDA; Semiconductor Integrated Circuit Device and Manufacture Thereof; Patent Abstracts of Japan; JP 10-229052; 08-25-1998; 14 Pages; Japan Patent Office	duplicate

Examiner Signature		Date Considered	10-31-5
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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